REMARKS

Claims 11 – 21 have been amended, claims 22-70 have been cancelled for possible pursuit in a divisional application and new claims 71 and 72 have been added. The application thus contains claims 1-21 and 71-72.

The Examiner objected to claims 11 and 12 and suggested more practical ways of expressing the subject matter on which applicant seeks a monopoly. Applicant wishes to thank the Examiner for the careful review of these claims and has adopted the Examiner's suggested wording.

35 USC 112

The Examiner rejected claims 12-21 under 35 USC 112 first paragraph as a single means claim.

35 USC 112 first paragraph states: "The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear concise and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same, and shall set forth the best mode contemplated by the inventor of carrying out his invention."

Claim 12 has been amended to recite:

12. An apparatus for encoding a plurality of predefined codes into a search key, the apparatus comprising a processor circuit and memory in communication with the processor circuit, said memory being configured to direct the processor circuit to:

    a) produce a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such

that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations, and

b) set bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes.

Claim 12 is now more clearly directed to a combination comprising a processor circuit and a memory configured to direct the processor circuit.

In view of the above it is respectfully submitted the rejection under 35 USC 112, first paragraph is overcome.

35 USC 102(b)

The Examiner has rejected claims 1-21 under 35 USC 102(b) as being anticipated by Srinivasan (Faster IP Lookups using Controlled Prefix Expansion, pages 1-10, ACM, June 1998).

Claim 1 recites:

"1. (Original) A method of encoding a plurality of predefined codes into a search key, the method comprising:

a) producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string having a length equal to or less than the longest predefined code in said plurality of said pre-defined codes such that said bit positions are arranged by the lengths of said possible bit combinations and by numeric value of said possible bit combinations; and

b) setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes."

Srinivasan fails to disclose "*producing a PNBA having a plurality of bit positions corresponding to possible bit combinations of a bit string...arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations and setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes.*

The Examiner relies on the disclosure at p.4, Figure 1 and the description on the left column related [to] prefix expansion, of Srinivasan for a description of the producing step recited in applicant's claim 1. Srinivasan however, at the location referenced by the Examiner, appears to disclose an expanded database of IP address prefixes wherein prefixes of fixed length are assigned to each original prefix. There is no disclosure of *producing a Prefix Node Bit Array (PNBA) having a plurality of bit positions corresponding to possible bit combinations of a bit string* as recited in applicant's claim 1. It is not clear what the Examiner regards as the Prefix Node Bit Array, nor what the Examiner regards as the plurality of bit positions in that array, nor what the Examiner regards as establishing a correspondence between a plurality of bit positions and possible bit combinations, nor what the Examiner regards as the arrangement of bit positions, as claimed in Applicant's claim 1.

The Examiner relies on the disclosure at p.4, Figure 1 and the description in the right column related [to] prefix capture, of Srinivasan for a description of the setting step recited in applicant's claim 1. Srinivasan however, at the location referenced by the Examiner, appears to disclose "picking from multiple copies of the same prefix such that when a low length prefix is expanded in length and one of its expansions "collides" with an existing prefix, then we say that the existing prefix captures the expansion prefix". When that happens Srinivasan suggests simply getting rid of the expansion prefix. The

expansion prefixes of Srinivasan, e.g. 11001, 10000, 10001, 1000001 and 1000000 for P8 = 1000000 cannot be said to even relate to the PNBA recited in applicant's claims because for one reason, the bit positions in the expansion prefixes of Srinivasan do not correspond to bit combinations identified by pre-defined codes, rather, the bit positions in any given prefix of Srinivasan appear to correspond to bit positions in an equivalent prefix of equal length. There is nothing that discloses or suggests *setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes,* as recited in applicant's claim 1. The Examiner is requested to take careful note of applicant's use of the terms "bit positions" and "possible bit combinations..." and the correspondence they have in applicant's claims. There is no teaching of any correspondence between a bit position and a bit combination in the Srinivasan reference.

From the foregoing, it is clear that Srinivasan fails to explicitly or inherently disclose or suggest each and every element of applicant's claim 1 in the combination claimed. Consequently applicant respectfully submits the rejection under 35 USC 102(b) is improper and should be withdrawn. Claim 1 is allowable over the Srinivasan reference.

Regarding claim 2, the Examiner states that at page 4, Figure 1; Srinivasan shows expanded prefixes are arranged bit positions (00-10000000) in order by ascending lengths (length 2 - length 7). Applicant's claim 2 recites:

2. (Original) The method claimed in claim 1 wherein producing comprises arranging said bit positions in order by ascending lengths of corresponding said possible bit combinations.

From the foregoing it would appear the Examiner considers the expanded prefixes of Srinivasan to be arranged bit positions. Claim 1, from which claim 2 depends recites producing a PNBA having bit positions...such that said bit positions are arranged...Claim 2 provides further specificity to what is meant

by "arranged". The Examiner's contention that the expanded prefixes are arranged bit positions, implies it is believed the expanded prefixes are equivalent to the PNBA recited in applicant's claim 1.

The arguments above in connection with Claim 1, explain that the expansion prefixes of Srinivasan are not equivalent to the PNBA recited in applicant's because for one reason, the bit positions in the expanded prefixes of Srinivasan do not correspond to possible bit combinations. Consequently, the expanded prefixes of Srinivasan are not the same "arranged bit positions" as recited by the present applicant since the bit positions of these expanded prefixes do not correspond to possible bit combinations. More particularly with reference to claim 2, the bit positions of the expanded prefixes of Srinivasan are not arranged in order by ascending lengths of corresponding said possible bit combinations, since the bits positions of these prefixes do not correspond to possible bit combinations....Consequently, the rejection of claim 2 under 35 USC 102(b) is improper.

Similar arguments apply in respect of claim 3 and therefore the rejection of claim 3 under 35 USC 102(b) is also improper.

Regarding claim 4, the Examiner suggests that Srinivasan further discloses producing [a] next hop array associating bit positions of said PNBA which have active bits with routing information for use by a router to route a packet. The Examiner relies on Figure 8, Link or Figure 9 (?) and pointer from root to leaves (?). Since Srinivasan has no Figures 8 or 9, applicant assumes the Examiner is referring to Tables 8 and 9. The term "Link" used by the Examiner is not understood in this context and the language "pointer from root to leaves" is not clear. Applicant respectfully requests the Examiner to clarify this rejection with reference to the specific page and column(s) of Srinivasan that explicitly or inherently describe the subject matter claimed by applicant in claim 4, or withdraw the rejection. In the meantime, applicant notes that claim 4 depends from claim 1 which has been shown to distinguish over Srinivasan

and therefore the rejection of claim 4 under 35 USC 102(b) is improper due to this dependence and due to the additional subject matter clamed in claim 4.

Regarding claim 5, the Examiner suggests that in addition to features recited in the base claim 1, Srinivasan further discloses "wherein producing comprises producing a plurality of PNBAs (expanded prefixes), each PNBA corresponding to a subgroup of bits of said predefined codes". The Examiner relies on Figure 8; expanded prefixes. Again, applicant assumes the reference to Figure 8 is a reference to Table 8. Table 8 is labeled "Memory Requirement (in K-Bytes) using the Variable Stride Dynamic Program, Non-leaf pushed and allowing packet array nodes. This Table appears to be simply an information Table with no supporting description in the text. Consequently, the Examiner's reference to Figure 8 is not understood. The Examiner's reference to expanded prefixes is assumed to be to the expanded prefixes shown above in connection with Figure 1 and an explanation has already been given to show that an expanded prefix is not the same as a PNBA as recited in applicant's claim. Therefore, since Srinivasan fails to disclose anything equivalent to a PNBA recited in applicant's claims, it would be improper to say that Srinivasan discloses producing a plurality of PNBAs as recited in claim 5. Therefore, the rejection of claim 5 under 35 USC 102(b) is improper due to its dependence upon claim 1 and due to the additional subject matter claimed in claim 5.

As for claims 6-10, each of these is ultimately dependent upon claim 5 and claim 1 and each of these further refines the features of the PNBA recited in claim 1. Since applicant has shown that Srinivasan fails to disclose the PNBA of claim 1, the rejection under 35 USC 102(b) as it pertains to each of claims 6-10 is improper due to this dependence and due to the additional subject matter claimed in each of these claims.

Claim 11 is a means language claim, following the language of claim 1 and therefore the arguments applied above in connection with claim 1 apply equally to claim 11. Thus, the rejection of claim 11 under 35 USC 102(b) is improper.

Claim 12 is a generic apparatus version of claim 1 and therefore the rejection of claim 12 under 35 USC 102(b) is improper for the same reasons as the rejection of claim 1.

Claims 13-21 are apparatus versions of claims 2-10 and therefore the rejections of these claims under 35 USC 102(b) are improper for the same reasons as the rejections of claims 2-10.

35 USC 102(e)

The Examiner has rejected claims 1-21 under 35 USC 102(e) as being anticipated by Srinivasan (US Patent No. 6,011,795). It is believed the reference to Srinivasan in connection with this patent is improper as it is conventional to refer to patents by the name of the first inventor, which in this patent is Varghese. It is noted however that the second inventor is Srinivasan and that the description of the invention in the Varghese patent is strikingly similar to the description in the Srinivasan article referenced above and both appear to be directed to the same idea; an idea which is quite different from applicant's claimed invention.

In connection with claim 1, the Examiner relies on columns 7 and 8, Figures 5-8 and the description related to prefix expansion of the Varghese patent for the producing step and relies on columns 8, Figures 5-8 and the description on the right column related to prefix capture for the setting step.

The particular areas of the Varghese patent relied on by the Examiner fail to explicitly or inherently teach *"producing a PNBA having a plurality of bit positions corresponding to possible bit combinations of a bit string...arranged by the lengths of said possible bit combinations and by numeric value of said bit combinations and setting bits active in bit positions which correspond to bit combinations of said possible bit combinations identified by said pre-defined codes.* As stated above in connection with the Srinivasan article, It is not clear what the Examiner regards as the Prefix Node Bit Array, nor what the

Examiner regards as the plurality of bit positions in that array, nor what the Examiner regards as establishing a correspondence between a plurality of bit positions and possible bit combinations, nor what the Examiner regards as the arrangement of bit positions, as claimed in Applicant's claim 1.

As for the setting step recited in applicant's claim 1, the Varghese patent, at the location referenced by the Examiner, appears to disclose "picking from multiple copies of the same prefix such that when a low length prefix is expanded in length and one of its expansions "collides" with an existing prefix, then we say that the existing prefix captures the expansion prefix, and simply getting rid of the expansion prefix". There is nothing that discloses or suggests that the bit positions in the expansion prefixes of Varghese should correspond to bit combinations identified by pre-defined codes, rather, the bit positions in any given prefix of Varghese appear to correspond to bit positions in an equivalent prefix of equal length. Again the Examiner is requested to take careful note of applicant's use of the terms "bit positions" and "possible bit combinations..." and the correspondence they have in applicant's claims. There is no teaching of any correspondence between a bit position and a bit combination in the Varghese reference.

From the foregoing, it is clear that Varghese fails to explicitly or inherently disclose or suggest each and every element of applicant's claim 1 in the combination claimed. Consequently applicant respectfully submits the rejection under 35 USC 102(e) is improper and should be withdrawn. Claim 1 is allowable over the Varghese reference.

Applicant respectfully submits that Claims 2-10 are ultimately dependent upon claim 1 and therefore the rejection of these claims under 35 USC 102(e) is improper due to this dependence and due to the additional subject matter each claims.

Claim 11 is a means language claim, following the language of claim 1 and therefore the arguments applied above in connection with claim 1 apply

equally to claim 11. Thus, the rejection of claim 11 under 35 USC 102(e) is improper.

Claim 12 is a generic apparatus version of claim 1 and therefore the rejection of claim 12 under 35 USC 102(e) is improper for the same reasons as the rejection of claim 1.

Claims 13-21 are apparatus versions of claims 2-10 and therefore the rejections of these claims under 35 USC 102(e) are improper for the same reasons as the rejections of claims 2-10.

Applicant respectfully requests further favorable consideration of the application.

Applicant hereby authorized the patent office to debit account No. 06-0713 in the amount of **$36.00** as payment of the excess claim fee for two additional dependent claims.

Respectfully submitted,

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